

UML/MARTE

Methodology

for Kista

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1 Introduction

Marte2Kista is a tool that enables the extraction of analysis models created with a UML tool and their direct analysis using the tool KISTA.

2 Model specification

2.1 Data Type

Two different kinds of data types are allowed: *PrimitiveType* and *DataType*. In this last case, the stereotype `<<DataSpecification>>` should be used for specifying the size of the data type, using the attribute *size*.

2.2 Application Components

The application components are modelled as *RtUnits* included in the *ApplicationView*. However, in this case, each *RtUnit* application component can have associated only one *File* (previously defined in the *FunctionalView*).

2.3 Concurrent Elements

The concurrent elements considered in the methodology are *SchedulableResource* components included in the *ConcurrencyView*. Each *SchedulableResource* component only can have a function that defines the functionality implemented by the concurrent element. Then, instances of these components define the static concurrency elements of the system.

These instances are characterized by the properties WCET, WCEI and WCME. These properties are annotated in a UML comment specified by the MARTE stereotype `<<RtSpecification>>`. In the attribute utility, these properties can be annotated as Figure 1.

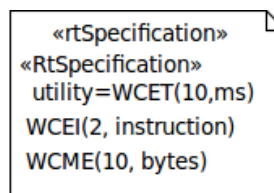


Figure 1 Definition of the WCET, WCEI and WCME properties

The notation is:

$WCET=(value, timeUnit); WCEI=(value, instruction); WCME=(value, bytes);$

Then, these *RtSpecification* comments are associated to each *SchedulableResource* instance by using UML links (Figure 2).

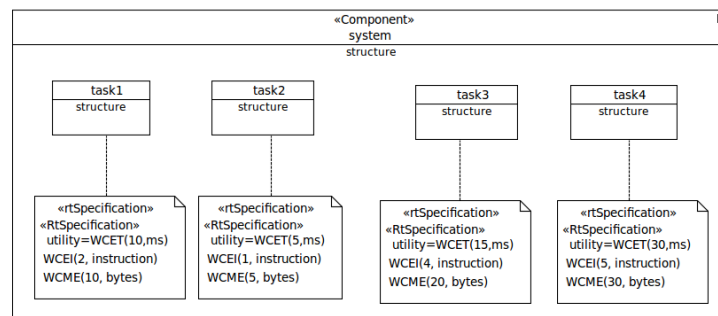


Figure 2 *Rtspecification* comments associated to *SchedulableResource* elements

Finally, these *RtSpecification* comments are owned by the System component of the *ConcurrencyView*.

2.4 HW communication resource

The HW resource used for modelling the communication in the HW platform must be a TDMA bus.

2.5 HW Processor

The HWProcessor components should behave the attribute assignedSlots.

2.6 Scheduling Policy

The Sw platform is defined by operating systems (OSs). These OSs are modelled by the stereotype <<OS>>. The scheduling policy associated to an *OS* component is defined by a UML component specified by the MARTE stereotype <<Scheduler>>. The scheduling policy is captured in the attributes *schedPolicy* and *otherSchedPolicy*.

The attribute *schedPolicy* is an enumeration. The possible values considered in this methodology are “EarliestDeadlineFirst”, “FixedPriority”, “RoundRobin”... “Other”.

In the case the value is “Other”, the scheduling policy is annotated in the attribute *otherSchedPolicy*.

In this attribute, two different styles can be considered. The first style is annotated the name of the policy. The names accepted are “static”, “DeadlineMonotonicScheduling”, “RateDeadline-MonotonicScheduling” ...

The second style is defining a set of properties. The properties are:

- policy. The accepted values are:
 - static
 - random
 - pseudoRandom
 - cycleExecutive
 - staticPriorities

- dynamicPriorities
- triggering. The accepted values are:
 - nonPreemptive
 - preemptive
 - cooperative
 - unknown
- timeSlice. The accepted values are:
 - no
 - yes
- dispatch. The accepted values are:
 - null
 - RateMonotonic or RM
 - EarliestDeadlineFirst or EDF

The second style, all the four properties should be annotated. Each value is separated by colon.

2.6.1 Static Policy

The concurrent elements are mapped on the operating systems (OSs) included in the definition of HW/SW platform of the *ArchitecturalView*. This mapping is captured by using UML abstraction specified by the MARTE stereotype <<Allocate>> (Figure 3).

In addition to that, the concurrent elements allocated in the same OS have to be scheduled, defining priority ordering. This priority ordering is annotated in UML constrained specified by the MARTE stereotype <<NfpConstraint>>. In this constraint, the priority ordering is annotated as:

$$\$schedulingOrder = nameConcurrentElement1, nameConcurrentElement2...$$

The order of the name involves the highest priority as the first concurrent element, and the lowest priority the last concurrent element. As a consequence of this ordering, all the channels where the application component mapped on the concurrent elements writes keep the same ordering.

The *NfpConstraint* is associated to the *OS* instance and the *NfpConstraints* are owned by the *System* element of the *ArchitecturalView* where the HW/SW platform is defined.

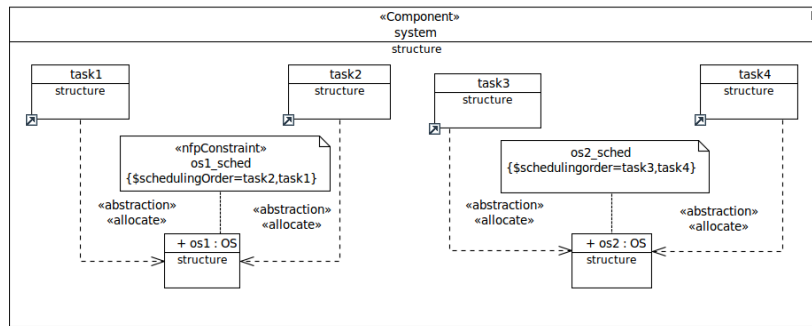


Figure 3 Concurrent elements mapping

When the bus used in the platform is a TDM, each processor connected to it has number of slots available for the communication. For capturing this property, a UML constraint specified by the MARTE stereotype <<NfpConstraint>> is used. In this *NfpConstraint*, this property is captured as:

$$\$numberOSslots = Integer$$

Then, the constraint is associated to a processor instance by using a UML link (Figure 4).

These constraints are owned by the *System* component included in the *ArchitecturalView*.

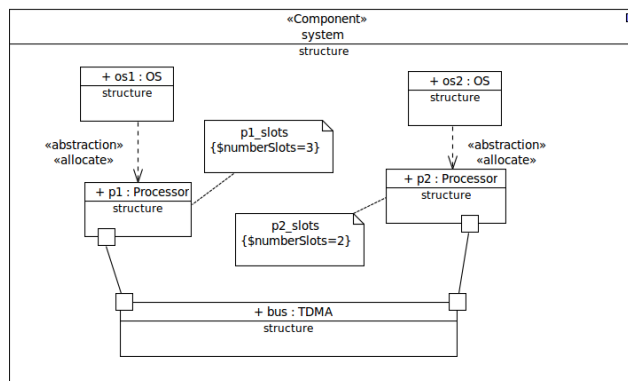


Figure 4 HW/SW platform with information about bus TDMA access

3 Annex I: Methodology Stereotypes

Stereotype	Attributes	Profile
RtSpecification	utility: Utility [0...1]	MARTE
OS	scheduler: Scheduler [1]	ESSYN
Scheduler	schedPolicy: SchedPolicyKind [1] otherSchedPolicy: String [0...1]	MARTE
NfpConstraint		MARTE
DataSpecification	size:NFP_Size [1]	ESSYN

4 Annexo II: Methodology Enumerations

Enumeration	Values	Profile
SchedPolicyKind	EarliestDeadlineFirst FIFO FixedPriority LeastLaxityFirst RoundRobin TimeTableDriven Undef Other	MARTE